AP

DOCKET NO.: 00-BN-051 (STMI01-00051) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Anthony X. Jarvis, et al.
Serial No.:	09/751,372
Filed:	December 29, 2000
For:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Group No.:	2183
Examiner:	Aimee J. Li

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicants herewith respectfully submit that the Examiner's decision of December 29, 2006, finally rejecting Claims 1-29 in the present application, should be reversed, in view of the following arguments and authorities. A check in the amount of $500.00 is enclosed for the fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

TABLE OF CONTENTS

TABLE OF AUTHORITIES iii
Real Party in Interest 4
Related Appeals or Interferences 4
Status of Claims 5
Status of Amendments after Final 6
SUMMARY OF CLAIMED SUBJECT MATTER 7
In General 7
Support for Independent Claims 7
Grounds of Rejection to be Reviewed on Appeal 11
1. Are Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to *Greenley et al.* ("Greenley") in view of U.S. Patent No. 5,706,481 to *Hannah, et al.* ("Hannah")? 11
ARGUMENT 12
Stated Grounds of Rejection 12
Legal Standards 12
Analysis of Examiner's Rejection 14
First Ground of Rejection 14
Grouping of Claims 63
REQUESTED RELIEF 64

APPENDIX A - Text of Claims on Appeal

APPENDIX B - Copy of Formal Drawings

APPENDIX C - Evidence Appendix

APPENDIX D - Related Proceedings Appendix

TABLE OF AUTHORITIES

Cases

Arkie Lures, Inc. v. Gene Larew Tackle, Inc., 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed.Cir. 1997) 11
In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993) 11
In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed.Cir. 1999) 12
In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992) 10
In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985) 11
In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992) 10, 11
In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993) 11
In re Rouffet, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed.Cir. 1998) 11, 12

Regulations

MPEP § 2142 ..... 10, 11

Real Party in Interest

The real party in interest, and assignee of this case, is STMicroelectronics, Inc. as indicated by:

an assignment recorded on May 7, 2001 in the Assignment Records of the United States Patent and Trademark Office at Reel 011769, Frame 0373;

an assignment recorded on August 2, 2001 in the Assignment Records of the United States Patent and Trademark Office at Reel 012044, Frame 0363; and

an assignment recorded on January 3, 2002 in the Assignment Records of the United States Patent and Trademark Office at Reel 012415, Frame 0370.

Related Appeals or Interferences

To the best knowledge and belief of the undersigned attorney, there are none.

Status of Claims

Claims 1-22 are under final rejection, and are each appealed.

Status of Amendments after Final

No claims were amended after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

In General

The present application is directed, in general, to data processors and, more specifically, to a data processor capable of executing load operations having different latencies. *Page 3, lines 7-9.*

Support for Independent Claims

Note that, per 37 CFR §41.37, only each of the independent claims are discussed in this section, as well as any claims including means-plus-function language that is argued separately below. In the arguments below, however, the dependent claims are also discussed and distinguished from the prior art. The discussion of the claims is for illustrative purposes, and is not intended to effect the scope of the claims.

Regarding Claim 1, a data processor 100 includes an instruction pipeline 400. (*Application, Page 24, Lines 20-22*). The pipeline 400 includes N processing stages 401-407. (*Application, Page 25, Lines 1-4*). Each of the processing stages 401-407 performs an execution step associated with a pending instruction being executed by the pipeline 400. (*Application, Page 25, Line 5 – Page 28, Line 8*). A data cache 330 is capable of storing data values used by the pending instruction. (*Application, Page 11, Lines 11-12; Page 28, Lines 13-19*). A plurality of registers 310 is capable of receiving the data values from the data cache 330. (*Application, Page 11, Lines 13-14; Page 27, Line*

22 – Page 28, Line 2). A load store unit 325 is capable of transferring a first data value from the data cache 330 to a target register during execution of a load operation. (*Application, Page 29, Line 8 – Page 30, Line 2*). A shifter circuit 535 is capable of shifting, sign extending, or zero extending the first data value prior to loading the first data value into the target register. (*Application, Page 29, Lines 17-22*). Bypass circuitry 530 is capable of transferring the first data value from the data cache 330 directly to the target register without processing the first data value in the shifter circuit 535. (*Application, Page 28, Line 20 – Page 29, Line 7*).

Regarding Claim 10, a method 600 for performing load operations in a data processor 100 is provided. (*Application, Page 29, Lines 8-10*). The method 600 includes determining if a pending instruction in an N-stage execution pipeline 400 is one of a load word operation, a load half-word operation, and a load byte operation. (*Application, Page 29, Lines 13-22*). If the pending instruction is a load half-word operation or a load byte operation, the method 600 includes transferring a first data value from a data cache 330 to a shifter circuit 535 and shifting the first data value prior to loading the first data value into a target register. (*Application, Page 29, Lines 10-13 and 17-22*). If the pending instruction is a load word operation, the method 600 includes transferring the first data value from the data cache 330 directly to the target register without processing the first data value in the shifter circuit 535. (*Application, Page 29, Lines 13-17*).

Regarding Claim 14, a processing system 10 includes a data processor 100, a memory 130, and a plurality of memory-mapped peripheral circuits 111-114 for performing selected functions. (*Application, Page 17, Lines 9-17*). The data processor 400 includes an instruction execution

pipeline 400 having N processing stages 401-407, each of which is capable of performing an execution step associated with a pending instruction being executed. (*Application, Page 24, Line 20 – Page 28, Line 8*). The data processor 400 also includes a data cache 330 capable of storing data values used by the pending instruction. (*Application, Page 11, Lines 11-12; Page 28, Lines 13-19*). The data processor 400 further includes a plurality of registers 310 capable of receiving the data values from the data cache 330. (*Application, Page 11, Lines 13-14; Page 27, Line 22 – Page 28, Line 2*). The data processor 400 also includes a load store unit 325 capable of transferring a first data value from the data cache 330 to a target register during execution of a load operation. (*Application, Page 29, Line 8 – Page 30, Line 2*). The data processor 400 further includes a shifter circuit 535 capable of shifting, sign extending, or zero extending the first data value prior to loading the first data value into the target register. (*Application, Page 29, Lines 17-22*). In addition, the data processor 400 includes bypass circuitry 530 capable of transferring the first data value from the data cache 330 directly to the target register without processing the first data value in the shifter circuit 535. (*Application, Page 28, Line 20 – Page 29, Line 7*).

With regard to claim 23, a data processor 400 also a data cache 330. (*Application, Page 11, Lines 7-12*). The data processor 400 further includes a plurality of registers 310 (*Application, Page 11*). The data processor 400 further includes a shifter circuit 535 capable of shifting, sign extending, or zero extending the first data value prior to loading the first data value into the target register. (*Application, Page 29, Lines 17-22*). In addition, the data processor 400 includes bypass circuitry 530 capable of transferring the first data value from the data cache 330 directly to the target register

without processing the first data value in the shifter circuit 535. (*Application, Page 28, Line 20 – Page 29, Line 7*).

With regard to claim 27, a method includes shifting, sign extending, or zero extending a first data value from a cache and providing a modified first data value to a first of a plurality of registers. (*Application, Page 29, Line 10 – Page 30, Line 2*). The method 600 includes transferring a second data value from the data cache 330 directly to the target register without shifting, sign extending, or zero extending the second data value. (*Application, Page 29, Lines 13-17*).

With regard to claim 29, a system 10 includes a processor 400. (*Application, Page 17, Lines 9-17*). The processor 400 includes a a cache 300. . (*Application, Page 11, Lines 11-12; Page 28, Lines 13-19*). The processor 400 includes a plurality of registers 310. (*Application, Page 11, Lines 13-14; Page 27, Line 22 – Page 28, Line 2*). The processor 400 includes a shifter circuit535 capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers (*Application, Page 29, Lines 17-22*). The processor 400 includes a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit (*Application, Page 28, Line 20 – Page 29, Line 7*). The system 10 includes a memory coupled 130 to the processor. (*Application, Page 17, Lines 9-17*). The system 10 includes a plurality of peripheral circuits 111-114 capable of performing selected functions in association with the processor. (*Application, Page 17, Lines 9-17*).

Grounds of Rejection to be Reviewed on Appeal

1. Are Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to *Greenley et al.* ("Greenley") in view of U.S. Patent No. 5,706,481 to *Hannah, et al.* ("Hannah")?

ARGUMENT

Stated Grounds of Rejection

The rejections outstanding against the Claims are as follows:

1. In the December 29, 2006 Office Action, Claims 1-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to *Greenley et al.* ("Greenley") in view of U.S. Patent No. 5,706,481 to *Hannah, et al.* ("Hannah").

Legal Standards

Obviousness: In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*. The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992; In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992; In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*. If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992; In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*.

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

In order to establish obviousness by combining references there must be some teaching or suggestion in the prior art to combine the references. *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed.Cir. 1997) ("It is insufficient to establish obviousness that the separate elements of an invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the references."); *In re Rouffet*, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed.Cir. 1998) ("When a rejection depends on a combination of prior art references, there must be some teaching, or motivation to combine the references.")

Evidence of a motivation to combine prior art references must be clear and particular if the trap of "hindsight" is to be avoided. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed.Cir. 1999) (Evidence of a suggestion, teaching or motivation to combine prior art references must be

"clear and particular." "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.'"). *In re Roufett*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed.Cir. 1998) ("[R]ejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'")

Analysis of Examiner's Rejection

First Ground of Rejection

Claims 1-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to *Greenley et al.* ("Greenley") in view of U.S. Patent No. 5,706,481 to *Hannah, et al.* ("Hannah").

Greenley recites a method and apparatus for improving the performance of pipelined processors. (*Abstract*). The apparatus of Greenley includes a data cache 180, an aligning unit 170, and a sign extension unit 160. (*Figure 1*). The aligning unit 170 aligns data retrieved from the data cache 180, and the sign extension unit 160 extends the sign of the retrieved data. (*Col. 2, Lines 32-54*). In particular, the aligning unit 170 right justifies the data retrieved from the data cache 180, and the sign extension unit 160 fills unoccupied bits with sign information. (*Col. 2, Lines 36-50*).

Hannah describes an apparatus and method for integrating texture memory and interpolation logic. Hannah describes "interpolator chains" in which certain portions of the "slices" can be

disabled. (*Col. 9,Llines 30-67*).

Claim 1

Independent claim 1 describes

1. A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

> bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

Claim 1 requires a "load store unit" capable of transferring a first data value from a "data cache" to a "target one of [a] plurality of registers" during execution of a load operation. Claim 1 also recites a "shifter circuit" capable of shifting, sign extending, or zero extending the first data value "prior to loading [the] first data value into [the] target register." In addition, Claims 1 and 14 recite "bypass circuitry" capable of "transferring [the] first data value from [the] data cache directly to [the] target register without processing [the] first data value in [the] shifter circuit."

Claims 1 is crystal clear – the "shifter circuit" can process a data value before the data value is loaded from a data cache into a target register. Also, the "bypass circuitry" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Examiner Li alleges that Greenley teaches

> A shifter circuit (Greenley 160,170 of Fig. 1) associated with said load store unit capable of one of a) shifting (Greenley Col.2 lines 19-31), b) sign extending (Greenley Col. 2 lines 48-54), and c) zero extending (Greenley Col. 2 lines 45-47) said first data value prior to

loading said first data value into said target register;

Examiner Li is incorrect; Greenley actually teaches, in col. 2, lines 19-54:

> Since needed data may not be physically stored consecutively in data cache 180, a LOAD access to data cache 180 must insure that the accessed data is aligned (i.e. both the upper and lower half of a word is fetched) into an appropriate format to write into a register in the register file 150. For example, when accessing a half-word from the data cache 180, the alignment unit 170 assures that the least significant bit of the half-word is in the least significant bit location in the register and the most significant bit of the half-word is in the bit position 15 in the register. After the word is aligned, it may be sign extended if the sign of the accessed word is ascertained during a signed load operation.
>
> Referring to FIG. 2, a detailed block diagram of the alignment unit 170 and the sign extension unit 160 coupled between the data cache 180 and a target register in the register file 150 is shown. The purpose of the alignment unit 170 is to right justify the data fetched from the data cache 180. For example, when a byte is fetched from the data cache 180, regardless of its byte position (i.e., 0 through 7) in the cache, the byte is always right justified in the alignment unit.

> Similarly, a half word is also right justified in the alignment unit 170, regardless of what position the half word occupied in the cache 180, or even if the two bytes of the half word were present in two different cache lines in the data cache 180. Words, double words, and extended words are similarly aligned by the alignment unit 170. In an unsigned load operation, the rest of the register not loaded with actual data is zero filled.
>
> The purpose of the sign extension unit 160 is to fill in the unoccupied bits of a register with sign information indicative of the sign of the data loaded from the data cache 180. The sign of the data is determined by its most significant bit ("MSB"). For example, if the MSB of the data is a "0", the data is considered positive. On the other hand, if the MSB is a "1", then the data is considered negative.

Examiner Li therefore claims that sign extension unit 160 and alignment unit 170 together form the claimed "shifter circuit." Examiner Li is correct in that sign extension unit 160 does perform sign extending, and the alignment unit 170 does perform zero filling and shifting. In fact, Greenley teaches that the alignment must be assured, and that alignment unit 170 assures that the appropriate bits of the half-words are in the appropriate bit positions. *See col. 2, lines 19-30.* It is clear from this that, in Greenley's system, that the "shifter circuit" of 160/170 cannot be bypassed, as

those functions must be present.

Examiner Li's position is therefore contradicted by the express recitations of Greenley. Regarding the aligning unit, Greenley specifically recites that load access to a data cache "must" insure that the accessed data is aligned. (*Col. 2, Lines 20-25*). Greenley also specifically recites that "double words" are "similarly aligned by the aligning unit." Regarding the sign extension unit, Greenley specifically recites that "double-words" are "similarly sign extended" by "the sign extension unit." (*Col. 2, Lines 60-61*).

It is clear, then, that Greenley does not, and cannot, include "bypass circuitry" as claimed, and Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

In Greenley, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Because of this, Greenley recites that all data passes through a shifter. More specifically, Greenley recites that all data passes through a shifter (the alignment unit 170 and the sign extension unit 160) before the data is stored in a register file 150.

Examiner Li instead references Hannah, and alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit (Hannah column 9, lines 31-67; Figure 11; Figure 12, Figure 13, and Figure 14)." This passage actually teaches:

FIG. 11 shows three examples of different configurations that can be used for the interpolator chains in the first configuration, four of the 4-bit unit 1101 can be stacked to perform 16-bit tri-linear interpolations. In the second configuration, a pair of the 8-bit unit 1102 can be stacked to perform the 16-bit tri-linear interpolations. In the third configuration, a single 12-bit unit 1103 is used to perform the interpolations. A number of multiplexers are programmed to couple the various units in order to achieve the desired configuration. In this manner, the same hardware can be utilized with minimal extra gate count to attain the flexibility in data width. In some applications, greater precision and resolution are desirable, whereas, in other applications, speed and cost are of greater importance.

In the currently preferred embodiment, the units 1101-1103 are comprised of an S-stage, a T-stage, and an LOD-stage. The S-stages are comprised of 4-bit slices 1104. The T-stages and LOD Stages are comprised of 6-bit slices 1105. These slices are designed to make the interpolators modular. FIG. 12 shows a basic 4-bit input interpolation slice.

> The data to the muxes comes from the subtractor (not shown). The most significant (MS) bits are either sign extension (if the slice is being used as the MS slice) or are the low order bits from the next more significant slice (when not the most significant slice). Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word. For example, for 8-bit texels, the MS slice would handle the sign bit (and no fraction bits) and the least significant (IS) slice would handle the fraction bits (but no sign). The slice configuration muxes separately enable or disable the slices MS portion (sign extension) or LS portion (fraction). FIG. 13 shows an 8-bit input interpolator, which is formed by coupling together two 4-bit slices. FIG. 14 shows a basic 6-bit input interpolator slice.

As is clear, at no point in this passage does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value from a data cache, as no data cache is shown or described here. One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transferred into a

target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value directly to a target register, as no registers are shown or described here. Hanna does not include any bypass circuitry that transfers any data values from a data cache to a register.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring the first data value without processing the first data value in a shifter circuit.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is associated with a load store unit.

Examiner Li does not even attempt to show where these limitations may be found within Hannah or these figures, and fails to allege even a single specific element that could meet the claim limitations. Indeed, this passage of Hannah appears to be cited simply because it includes the term "bypassed". The particular sentence of Hannah the Examiner reiterates in response is "Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word." The Examiner then acknowledges that Hannah doesn't actually teach any bypass circuitry, stating:

> Hannah also teaches in column 9, lines 37-44 that his implementation of the multiplexers he minimizes gate count, e.g. reduce the size of

> the device, and attains "flexibility in data width." Hannah then proceeds to state that "In some applications greater precision and resolution are desirable, whereas, in other applications, speed and cost are of greater importance." This suggests that how the multiplexers are used, e.g. to bypass certain capabilities, dependent on the designers desire. Bypassing effectively disables a functionality, such as the sign extension mentioned in both Greenley and Hannah, so that it is not performed and time is not wasted on an unneeded functionality. Consequently, the speed is increased in the system.

The Examiner does not – and tacitly admits that she cannot – identify any specific circuit in Hannah that is a bypass circuitry associated with a load store unit capable of transferring a first data value from a data cache directly to a target register without processing the first data value in a shifter circuit, as claimed. To the extent anything in Hannah is bypassed at all, there is no "bypass circuitry" connected as claimed or capable of performing the claimed functions.

Examiner Li alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit." Examiner Li is incorrect -- no data cache is shown or described here, as required by the claims, and as Examiner Li attempts to ignore by simply referencing a "target". One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which

are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transfer into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

Examiner Li therefore fails to make a *prima facie* obviousness rejection. Even if there were motivation to combine these references, the proposed combination still does not include the claim limitations.

Since Greenley does not teach or suggest the claimed features, and Hannah does not teach or suggest the claimed features, no combination of these references can teach or suggest the claimed features. As these features are found in all independent claims, all claims distinguish over Greenley, Hannah, and any combination of them. Greenley, in fact, teaches away from the Examiner's proposed combination and further modification by teaching that the shift functions must be used for any data transfer.

Applicant further notes that the Examiner Li's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of the passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping. There is no proper motivation in the reference itself, explicitly or implicitly, nor in the knowledge of one of ordinary skill in the art, nor in the problem to be solved.

The rejection of this claim should be reversed.

Claim 2

Claim 2 requires, among other limitations, that "said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 2 depends from claim 1; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference.

Examiner Li does not make any attempt to show this limitation in the art, and so fails to make a *prima facie* rejection. The Examiner simply asserts that "Greenley's loading of a double word has the same consequences as applicant's loading of a word." Even if this were true, it is irrelevant – the Examiner is required to show that the claim limitation itself is taught in some reference, and the Examiner cannot.

As Greenley doesn't even include bypass circuitry, as the Examiner admits, the Examiner's reliance on Greeley for a limitation relating to the operation of the bypass circuitry is particularly empty. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being performed during a load word operation.

The rejection of this claim should be reversed.

Claim 3

Claim 3 requires, among other limitations, that "bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 3 depends from claim 2; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner again relies on Greenley to teach this limitation. As Greenley doesn't even include bypass circuitry, as the Examiner admits, the Examiner's reliance on Greeley for a limitation relating to the operation of the bypass circuitry is particularly empty. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being performed during a load word operation, and at the end of two machine cycles.

The rejection of this claim should be reversed.

Claim 4

Claim 4 requires, among other limitations, that "shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 4 depends from claim 1; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference. The rejection of this claim should be reversed.

Claim 5

Claim 5 requires, among other limitations, that the "shifter circuit loads said shifted first data value into said target register at the end of three machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 5 depends from claim 4; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner makes no showing in the art of this limitation. Instead, the Examiner hypothesizes what latency savings might occur in the proposed combination, without making any reference to the teachings of the art itself, and then indicates that the claim limitation is simply a "change in magnitude of latency" over a hypothesis based on a proposed combination. The limitation is not taught or suggested by the art of record, alone or in combination, and the Examiner cannot make a showing of any actual relevant teaching in the art.

The rejection of this claim should be reversed.

Claim 6

Claim 6 requires, among other limitations, that "shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 6 depends from claim 1; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference. The rejection of this claim should be reversed.

Claim 7

Claim 7 requires, among other limitations, that the "shifter circuit loads said shifted first data value into said target register at the end of three machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 7 depends from claim 6, therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner makes no showing in the art of this limitation. Instead, the Examiner hypothesizes what latency savings might occur in the proposed combination, without making any reference to the teachings of the art itself, and then indicates that the claim limitation is simply a

"change in magnitude of latency" over a hypothesis based on a proposed combination. The limitation is not taught or suggested by the art of record, alone or in combination, and the Examiner cannot make a showing of any actual relevant teaching in the art.

The rejection of this claim should be reversed.

Claim 8

Claim 8 requires, among other limitations, that the "bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 8 depends from claim 1; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference.

As described above, neither reference teaches the claimed bypass circuitry. The Examiner does not even attempt to show that this limitation is met, and so fails to make even a *prima facie* obviousness rejection. Instead, the Examiner simply alleges that Hannah has a multiplexer with an input channel coupled to "an output of another device".

This is not the claim limitation. Hannah does not teach or suggest the claim limitation. Virtually any multiplexer input is connected to an output of something, but that is not enough to teach or suggest the limitations of the claim.

The rejection of this claim should be reversed.

Claim 9

Claim 9 requires, among other limitations, that the "multiplexer has a second input channel coupled to an output of said shifter circuit."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 9 depends from claim 8; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

As described above, neither reference teaches the claimed bypass circuitry. The Examiner does not even attempt to show that this limitation is met, and so fails to make even a *prima facie* obviousness rejection. Instead, the Examiner simply alleges that Hannah has a multiplexer with an input channel coupled to "an output of another device".

This is not the claim limitation. Hannah does not teach or suggest the claim limitation. Virtually any multiplexer input is connected to an output of something, but that is not enough to teach or suggest the limitations of the claim.

As can be seen, with respect to Claims 8 and 9, the Examiner has not shown any multiplexer connected as required, and has not even alleged any teaching corresponding to these claim limitations.

The rejection of this claim should be reversed.

Claim 10

Independent claim 10 describes

> 10. A method of loading a first data value from a data cache into a target register of a plurality of registers, the method comprising the steps of:
>
> determining if a pending instruction in an N-stage execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation;
>
> in response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register;
>
> in response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to the shifter circuit and shifting the first data value prior to loading the first data value into the target register; and
>
> in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit.

Claim 10 requires "transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit." This limitation is not taught or suggested by the art of record. The Examiner alleges that this is taught by Greenly at col. 2, lines 35-40, but the Examiner is mistaken:

> The purpose of the alignment unit 170 is to right justify the data fetched from the data cache 180. For example, when a byte is fetched from the data cache 180, regardless of its byte position (i.e., 0 through 7) in the cache, the byte is always right justified in the alignment unit.

It is clear that the passage on which the Examiner relies does not teach or suggest anything at all related to the claim limitation.

Further, neither Greenley or Hannah teach or suggest doing anything in response to a determination that a pending instruction is a load word operation as recited in Claim 10. The Examiner's rejection on this point repeats both the combination above and the motivation addressed below, neither of which teach or suggest anything at all with respect to this particular limitation. As the BPAI has noted recently in cases such as *Ex Parte Rinkevich et al.* (BPAI 2007-1317), a consideration of when processes occur in response to other actions can illustrate a patentable distinction.

The rejection of this claim should be reversed.

Claim 11

Claim 11 requires, among other limitations, that "the step of transferring the first data value requires two machine cycles during a load word operation."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 11 depends from claim 10; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner again relies on Greenley to teach this limitation. Greenley doesn't even the direct transfer of the parent claim. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being performed during a load word operation, and requiring two machine cycles.

The rejection of this claim should be reversed.

Claim 12

Claim 12 requires, among other limitations, that "the step of transferring the first data value requires three machine cycles during a load half-word operation."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 12 depends from claim 10; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner makes no showing in the art of this limitation. Instead, the Examiner hypothesizes what latency savings might occur in the proposed combination, without making any reference to the teachings of the art itself, and then indicates that the claim limitation is simply a "change in magnitude of latency" over a hypothesis based on a proposed combination. The limitation is not taught or suggested by the art of record, alone or in combination, and the Examiner cannot make a showing of any actual relevant teaching in the art.

The rejection of this claim should be reversed.

Claim 13

Claim 13 requires, among other limitations, that "the step of transferring the first data value requires three machine cycles during a load byte operation."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 13 depends from claim 10; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner makes no showing in the art of this limitation. Instead, the Examiner hypothesizes what latency savings might occur in the proposed combination, without making any reference to the teachings of the art itself, and then indicates that the claim limitation is simply a "change in magnitude of latency" over a hypothesis based on a proposed combination. The limitation is not taught or suggested by the art of record, alone or in combination, and the Examiner

cannot make a showing of any actual relevant teaching in the art.

The rejection of this claim should be reversed.

Claim 14

Independent claim 14 describes

> 14. A processing system comprising:
>
> a data processor comprising:
>
> an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;
>
> a data cache capable of storing data values used by said pending instruction;
>
> a plurality of registers capable of receiving said data values from said data cache;
>
> a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;
>
> a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first

data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit;

a memory coupled to said data processor; and

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

Claim 14 requires a "load store unit" capable of transferring a first data value from a "data cache" to a "target one of [a] plurality of registers" during execution of a load operation. Claim 14 also recites a "shifter circuit" capable of shifting, sign extending, or zero extending the first data value "prior to loading [the] first data value into [the] target register." In addition, Claim 14 recites "bypass circuitry" capable of "transferring [the] first data value from [the] data cache directly to [the] target register without processing [the] first data value in [the] shifter circuit."

Claim 14 is clear that the "shifter circuit" can process a data value before the data value is loaded from a data cache into a target register. Also, the "bypass circuitry" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Examiner Li alleges that Greenley teaches

> A shifter circuit (Greenley 160,170 of Fig. 1) associated with said load store unit capable of one of a) shifting (Greenley Col.2 lines 19-31), b) sign extending (Greenley Col. 2 lines 48-54), and c) zero extending (Greenley Col. 2 lines 45-47) said first data value prior to loading said first data value into said target register;

Examiner Li is incorrect. The passage cited by the Examiner is reproduced above with relation to claim 1, and does not teach or suggest that which the Examiner alleges.

Examiner Li claims that sign extension unit 160 and alignment unit 170 together form the claimed "shifter circuit." Examiner Li is correct in that sign extension unit 160 does perform sign extending, and the alignment unit 170 does perform zero filling and shifting. In fact, Greenley teaches that the alignment must be assured, and that alignment unit 170 assures that the appropriate bits of the half-words are in the appropriate bit positions. *See col. 2, lines 19-30.* It is clear from this that, in Greenley's system, that the "shifter circuit" of 160/170 cannot be bypassed, as those functions must be present.

Examiner Li's position is therefore contradicted by the express recitations of Greenley. Regarding the aligning unit, Greenley specifically recites that load access to a data cache "must" insure that the accessed data is aligned. (*Col. 2, Lines 20-25*). Greenley also specifically recites that "double words" are "similarly aligned by the aligning unit." Regarding the sign extension unit, Greenley specifically recites that "double-words" are "similarly sign extended" by "the sign

extension unit." (*Col. 2, Lines 60-61*).

It is clear, then, that Greenley does not, and cannot, include "bypass circuitry" as claimed, and Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

In Greenley, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Because of this, Greenley recites that all data passes through a shifter. More specifically, Greenley recites that all data passes through a shifter (the alignment unit 170 and the sign extension unit 160) before the data is stored in a register file 150.

Examiner Li instead references Hannah, and alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit (Hannah column 9, lines 31-67; Figure 11; Figure 12, Figure 13, and Figure 14)." As reproduced above with relation to claim 1, this passage of Hannah teaches nothing of the sort.

At no point in this passage does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value from a data cache, as no data cache is shown or described here. One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transferred into a target register, as

required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value directly to a target register, as no registers are shown or described here. Hanna does not include any bypass circuitry that transfers any data values from a data cache to a register.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring the first data value without processing the first data value in a shifter circuit.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is associated with a load store unit.

Examiner Li does not even attempt to show where these limitations may be found within Hannah or these figures, and fails to allege even a single specific element that could meet the claim limitations. Indeed, this passage of Hannah appears to be cited simply because it includes the term "bypassed". The particular sentence of Hannah the Examiner reiterates in response is "Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word." The Examiner then acknowledges that Hannah doesn't actually teach any bypass circuitry, and simply states that Hannah's description "suggests" that the multiplexers are used to bypass certain capabilities

The Examiner does not – and tacitly admits that she cannot – identify any specific circuit in

Hannah that is a bypass circuitry associated with a load store unit capable of transferring a first data value from a data cache directly to a target register without processing the first data value in a shifter circuit, as claimed. To the extent anything in Hannah is bypassed at all, there is no "bypass circuitry" connected as claimed or capable of performing the claimed functions.

Examiner Li alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit." Examiner Li is incorrect -- no data cache is shown or described here, as required by the claims, and as Examiner Li attempts to ignore by simply referencing a "target". One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transfer into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

Examiner Li therefore fails to make a *prima facie* obviousness rejection. Even if there were motivation to combine these references, the proposed combination still does not include the claim limitations.

Since Greenley does not teach or suggest the claimed features, and Hannah does not teach or suggest the claimed features, no combination of these references can teach or suggest the claimed features. As these features are found in all independent claims, all claims distinguish over Greenley, Hannah, and any combination of them. Greenley, in fact, teaches away from the Examiner's

proposed combination and further modification by teaching that the shift functions must be used for any data transfer.

Applicant further notes that the Examiner Li's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of the passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping. There is no proper motivation in the reference itself, explicitly or implicitly, nor in the knowledge of one of ordinary skill in the art, nor in the problem to be solved.

The rejection of this claim should be reversed.

Claim 15

Claim 15 requires, among other limitations, that "said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 15 depends from claim 14; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference.

Examiner Li does not make any attempt to show this limitation in the art, and so fails to make a *prima facie* rejection. The Examiner simply asserts that "Greenley's loading of a double word has

the same consequences as applicant's loading of a word." Even if this were true, it is irrelevant – the Examiner is required to show that the claim limitation itself is taught in some reference, and the Examiner cannot.

As Greenley doesn't even include bypass circuitry, as the Examiner admits, the Examiner's reliance on Greeley for a limitation relating to the operation of the bypass circuitry is particularly empty. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being performed during a load word operation.

The rejection of this claim should be reversed.

Claim 16

Claim 16 requires, among other limitations, that "bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 16 depends from claim 15; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner again relies on Greenley to teach this limitation. As Greenley doesn't even include bypass circuitry, as the Examiner admits, the Examiner's reliance on Greeley for a limitation relating to the operation of the bypass circuitry is particularly empty. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being

performed during a load word operation, and at the end of two machine cycles.

The rejection of this claim should be reversed.

Claim 17

Claim 17 requires, among other limitations, that "shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 17 depends from claim 14; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference. The rejection of this claim should be reversed.

Claim 18

Claim 18 requires, among other limitations, that the "shifter circuit loads said shifted first data value into said target register at the end of three machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 18 depends from claim 17; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner makes no showing in the art of this limitation. Instead, the Examiner hypothesizes what latency savings might occur in the proposed combination, without making any reference to the teachings of the art itself, and then indicates that the claim limitation is simply a "change in magnitude of latency" over a hypothesis based on a proposed combination. The limitation is not taught or suggested by the art of record, alone or in combination, and the Examiner cannot make a showing of any actual relevant teaching in the art.

The rejection of this claim should be reversed.

Claim 19

Claim 19 requires, among other limitations, that "shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 19 depends from claim 14; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference. The rejection of this claim should be reversed.

Claim 20

Claim 20 requires, among other limitations, that the "shifter circuit loads said shifted first

data value into said target register at the end of three machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 20 depends from claim 19, therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner makes no showing in the art of this limitation. Instead, the Examiner hypothesizes what latency savings might occur in the proposed combination, without making any reference to the teachings of the art itself, and then indicates that the claim limitation is simply a "change in magnitude of latency" over a hypothesis based on a proposed combination. The limitation is not taught or suggested by the art of record, alone or in combination, and the Examiner cannot make a showing of any actual relevant teaching in the art.

The rejection of this claim should be reversed.

Claim 21

Claim 21 requires, among other limitations, that the "bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 21 depends from claim 14; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference.

As described above, neither reference teaches the claimed bypass circuitry. The Examiner does not even attempt to show that this limitation is met, and so fails to make even a *prima facie* obviousness rejection. Instead, the Examiner simply alleges that Hannah has a multiplexer with an input channel coupled to "an output of another device".

This is not the claim limitation. Hannah does not teach or suggest the claim limitation. Virtually any multiplexer input is connected to an output of something, but that is not enough to teach or suggest the limitations of the claim.

The rejection of this claim should be reversed.

Claim 22

Claim 22 requires, among other limitations, that the "multiplexer has a second input channel coupled to an output of said shifter circuit."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 22 depends from claim 21; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

As described above, neither reference teaches the claimed bypass circuitry. The Examiner does not even attempt to show that this limitation is met, and so fails to make even a *prima facie* obviousness rejection. Instead, the Examiner simply alleges that Hannah has a multiplexer with an input channel coupled to "an output of another device".

This is not the claim limitation. Hannah does not teach or suggest the claim limitation. Virtually any multiplexer input is connected to an output of something, but that is not enough to teach or suggest the limitations of the claim.

As can be seen, with respect to Claims 21 and 22, the Examiner has not shown any multiplexer connected as required, and has not even alleged any teaching corresponding to these claim limitations.

The rejection of this claim should be reversed.

Claim 23

Independent claim 23 requires:

> 23. A processor, comprising:
>
> a cache;
>
> a plurality of registers;
>
> a shifter circuit capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers; and
>
> a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit.

Claim 23 recites a "shifter circuit" capable of shifting, sign extending, or zero extending a

data value from the cache and providing a modified data value to a target one of the registers. In addition, Claim 23 recites a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit.

Claim 23 is clear that "bypass circuit" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Examiner Li alleges that Greenley teaches

> A shifter circuit (Greenley 160,170 of Fig. 1) associated with said load store unit capable of one of a) shifting (Greenley Col.2 lines 19-31), b) sign extending (Greenley Col. 2 lines 48-54), and c) zero extending (Greenley Col. 2 lines 45-47) said first data value prior to loading said first data value into said target register;

Examiner Li is incorrect. The passage cited by the Examiner is reproduced above with relation to claim 1, and does not teach or suggest that which the Examiner alleges.

Examiner Li claims that sign extension unit 160 and alignment unit 170 together form the claimed "shifter circuit." Examiner Li is correct in that sign extension unit 160 does perform sign extending, and the alignment unit 170 does perform zero filling and shifting. In fact, Greenley teaches that the alignment must be assured, and that alignment unit 170 assures that the appropriate bits of the half-words are in the appropriate bit positions. *See col. 2, lines 19-30.* It is clear from this that, in Greenley's system, that the "shifter circuit" of 160/170 cannot be bypassed, as those

functions must be present.

Examiner Li's position is therefore contradicted by the express recitations of Greenley. Regarding the aligning unit, Greenley specifically recites that load access to a data cache "must" insure that the accessed data is aligned. (*Col. 2, Lines 20-25*). Greenley also specifically recites that "double words" are "similarly aligned by the aligning unit." Regarding the sign extension unit, Greenley specifically recites that "double-words" are "similarly sign extended" by "the sign extension unit." (*Col. 2, Lines 60-61*).

It is clear, then, that Greenley does not, and cannot, include "bypass circuitry" as claimed, and Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

In Greenley, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Because of this, Greenley recites that all data passes through a shifter. More specifically, Greenley recites that all data passes through a shifter (the alignment unit 170 and the sign extension unit 160) before the data is stored in a register file 150.

Examiner Li instead references Hannah, and alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit (Hannah column 9, lines 31-67; Figure 11; Figure 12, Figure 13, and Figure 14)." As reproduced above with relation to claim 1, this passage of Hannah teaches nothing of the sort.

At no point in this passage does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value from a data cache, as no data cache is shown or described here. One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transferred into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value directly to a target register, as no registers are shown or described here. Hanna does not include any bypass circuitry that transfers any data values from a data cache to a register.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring the first data value without processing the first data value in a shifter circuit.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is associated with a load store unit.

Examiner Li does not even attempt to show where these limitations may be found within Hannah or these figures, and fails to allege even a single specific element that could meet the claim limitations. Indeed, this passage of Hannah appears to be cited simply because it includes the term

"bypassed". The particular sentence of Hannah the Examiner reiterates in response is "Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word." The Examiner then acknowledges that Hannah doesn't actually teach any bypass circuitry, and simply states that Hannah's description "suggests" that the multiplexers are used to bypass certain capabilities

The Examiner does not – and tacitly admits that she cannot – identify any specific circuit in Hannah that is a bypass circuitry associated with a load store unit capable of transferring a first data value from a data cache directly to a target register without processing the first data value in a shifter circuit, as claimed. To the extent anything in Hannah is bypassed at all, there is no "bypass circuitry" connected as claimed or capable of performing the claimed functions.

Examiner Li alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit." Examiner Li is incorrect -- no data cache is shown or described here, as required by the claims, and as Examiner Li attempts to ignore by simply referencing a "target". One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transfer into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

Examiner Li therefore fails to make a *prima facie* obviousness rejection. Even if there were

motivation to combine these references, the proposed combination still does not include the claim limitations.

Since Greenley does not teach or suggest the claimed features, and Hannah does not teach or suggest the claimed features, no combination of these references can teach or suggest the claimed features. As these features are found in all independent claims, all claims distinguish over Greenley, Hannah, and any combination of them. Greenley, in fact, teaches away from the Examiner's proposed combination and further modification by teaching that the shift functions must be used for any data transfer.

Applicant further notes that the Examiner Li's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of the passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping. There is no proper motivation in the reference itself, explicitly or implicitly, nor in the knowledge of one of ordinary skill in the art, nor in the problem to be solved.

The rejection of this claim should be reversed.

Claim 24

Claim 24 requires, among other limitations, that "the data value is transferred from the cache to the target register via the bypass circuit during a load word operation."

This limitation, in combination with the limitations of the parent claim, is not taught or suggested by any art of record, alone or in combination.

Claim 24 depends from claim 23; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference.

Examiner Li does not make any attempt to show this limitation in the art, and so fails to make a *prima facie* rejection. The Examiner simply asserts that "Greenley's loading of a double word has the same consequences as applicant's loading of a word." Even if this were true, it is irrelevant – the Examiner is required to show that the claim limitation itself is taught in some reference, and the Examiner cannot.

As Greenley doesn't even include bypass circuitry, as the Examiner admits, the Examiner's reliance on Greeley for a limitation relating to the operation of the bypass circuitry is particularly empty. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being performed during a load word operation.

The rejection of this claim should be reversed.

Claim 25

Claim 25 requires, among other limitations, that "the bypass circuit is capable of transferring the data value from the cache to the target register at an end of two machine cycles; and the shifter circuit is capable of providing the modified data value to the target register at an end of three machine cycles."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 25 depends from claim 24; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

The Examiner again relies on Greenley to teach this limitation. As Greenley doesn't even include bypass circuitry, as the Examiner admits, the Examiner's reliance on Greeley for a limitation relating to the operation of the bypass circuitry is particularly empty. This particular transfer operation is not taught or suggested by any art of record, and certainly is not taught as being performed during a load word operation, and at the end of two machine cycles.

The rejection of this claim should be reversed.

Claim 26

Claim 26 requires, among other limitations, that the "bypass circuit comprises a multiplexer having a first input coupled to the cache and a second input coupled to the shifter circuit."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 26 depends from claim 23; therefore the arguments above with respect to the parent claim apply here as well, and are hereby incorporated by reference.

As described above, neither reference teaches the claimed bypass circuitry. The Examiner simply makes general reference to a passage of Hannah reproduced above and refers to several of

Hannah's figures. None of these depicts the claimed bypass circuitry. The Examiner completely fails to show any multiplexer in Hannah connected as claimed, and doesn't bother to identify any specific element at all.

The rejection of this claim should be reversed.

Claim 27

Independent claim 27 provides:

> 27. A method, comprising:
>
> shifting, sign extending, or zero extending a first data value from a cache and providing a modified first data value to a first of a plurality of registers; and
>
> transferring a second data value from the cache to a second of the plurality of registers without shifting, sign extending, or zero extending the second data value.

Claim 27 requires transferring a second data value from the cache to a second of the plurality of registers without shifting, sign extending, or zero extending the second data value." This limitation is not taught or suggested by the art of record. The Examiner alleges that this is taught by Greenley, but the Examiner is mistaken.

It is clear that the passages on which the Examiner relies do not teach or suggest anything at all related to the claim limitation.

The rejection of this claim should be reversed.

Claim 28

Claim 28 requires, among other limitations, "transferring the second data value comprises transferring the second data value to the second register in response to determining that a second pending instruction in the processor is a load word operation."

This limitation, in combination with the limitations of the parent claims, is not taught or suggested by any art of record, alone or in combination.

Claim 28 depends from claim 27; therefore the arguments above with respect to the parent claims apply here as well, and are hereby incorporated by reference.

Neither Greenley or Hannah teach or suggest doing anything in response to determining that a second pending instruction in the processor is a load word operation as recited in Claim 28. The Examiner's rejection on this point repeats both the combination above and the motivation addressed below, neither of which teach or suggest anything at all with respect to this particular limitation. As the BPAI has noted recently, a consideration of when processes occur in response to other actions can illustrate a patentable distinction.

The rejection of this claim should be reversed.

Claim 29

Independent Claim 29 describes:

29. A system, comprising:

a processor comprising:

a cache;

a plurality of registers;

a shifter circuit capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers; and

a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit;

a memory coupled to the processor; and

a plurality of peripheral circuits capable of performing selected functions in association with the processor.

Claim 29 recites a "shifter circuit" capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers. In addition, Claim 29 recites a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit.

Claim 29 is clear that "bypass circuit" can transfer the data value from the data cache directly

to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Examiner Li alleges that Greenley teaches

> A shifter circuit (Greenley 160,170 of Fig. 1) associated with said load store unit capable of one of a) shifting (Greenley Col.2 lines 19-31), b) sign extending (Greenley Col. 2 lines 48-54), and c) zero extending (Greenley Col. 2 lines 45-47) said first data value prior to loading said first data value into said target register;

Examiner Li is incorrect. The passage cited by the Examiner is reproduced above with relation to claim 1, and does not teach or suggest that which the Examiner alleges.

Examiner Li claims that sign extension unit 160 and alignment unit 170 together form the claimed "shifter circuit." Examiner Li is correct in that sign extension unit 160 does perform sign extending, and the alignment unit 170 does perform zero filling and shifting. In fact, Greenley teaches that the alignment must be assured, and that alignment unit 170 assures that the appropriate bits of the half-words are in the appropriate bit positions. *See col. 2, lines 19-30.* It is clear from this that, in Greenley's system, that the "shifter circuit" of 160/170 cannot be bypassed, as those functions must be present.

Examiner Li's position is therefore contradicted by the express recitations of Greenley. Regarding the aligning unit, Greenley specifically recites that load access to a data cache "must" insure that the accessed data is aligned. (*Col. 2, Lines 20-25*). Greenley also specifically recites that

"double words" are "similarly aligned by the aligning unit." Regarding the sign extension unit, Greenley specifically recites that "double-words" are "similarly sign extended" by "the sign extension unit." (*Col. 2, Lines 60-61*).

It is clear, then, that Greenley does not, and cannot, include "bypass circuitry" as claimed, and Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

In Greenley, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Because of this, Greenley recites that all data passes through a shifter. More specifically, Greenley recites that all data passes through a shifter (the alignment unit 170 and the sign extension unit 160) before the data is stored in a register file 150.

Examiner Li instead references Hannah, and alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit (Hannah column 9, lines 31-67; Figure 11; Figure 12, Figure 13, and Figure 14)." As reproduced above with relation to claim 1, this passage of Hannah teaches nothing of the sort.

At no point in this passage does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value from a data cache, as no data cache is shown or described here. One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output

samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transferred into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value directly to a target register, as no registers are shown or described here. Hanna does not include any bypass circuitry that transfers any data values from a data cache to a register.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring the first data value without processing the first data value in a shifter circuit.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is associated with a load store unit.

Examiner Li does not even attempt to show where these limitations may be found within Hannah or these figures, and fails to allege even a single specific element that could meet the claim limitations. Indeed, this passage of Hannah appears to be cited simply because it includes the term "bypassed". The particular sentence of Hannah the Examiner reiterates in response is "Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word." The Examiner then acknowledges that Hannah doesn't actually teach any bypass circuitry, and simply states that

Hannah's description "suggests" that the multiplexers are used to bypass certain capabilities

The Examiner does not – and tacitly admits that she cannot – identify any specific circuit in Hannah that is a bypass circuitry associated with a load store unit capable of transferring a first data value from a data cache directly to a target register without processing the first data value in a shifter circuit, as claimed. To the extent anything in Hannah is bypassed at all, there is no "bypass circuitry" connected as claimed or capable of performing the claimed functions.

Examiner Li alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit." Examiner Li is incorrect -- no data cache is shown or described here, as required by the claims, and as Examiner Li attempts to ignore by simply referencing a "target". One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transfer into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

Examiner Li therefore fails to make a *prima facie* obviousness rejection. Even if there were motivation to combine these references, the proposed combination still does not include the claim limitations.

Since Greenley does not teach or suggest the claimed features, and Hannah does not teach or suggest the claimed

features. As these features are found in all independent claims, all claims distinguish over Greenley, Hannah, and any combination of them. Greenley, in fact, teaches away from the Examiner's proposed combination and further modification by teaching that the shift functions must be used for any data transfer.

Applicant further notes that the Examiner Li's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of the passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping. There is no proper motivation in the reference itself, explicitly or implicitly, nor in the knowledge of one of ordinary skill in the art, nor in the problem to be solved.

The rejection of this claim should be reversed.

All rejections are traversed, and should be reversed.

Applicant further notes that the Examiner's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of a passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping.

Other distinctions remain, but need not be addressed at this time, as all claims are shown to

distinguish over the art of record, alone or in combination.

Grouping of Claims

The claims on appeal do not stand or fall together, as may be seen from the arguments set forth below. Each claim has been argued separately under a separate subheading, and each claim should be considered separately. While the applicant recognizes that a formal statement regarding the grouping of claims is no longer required, each claim should be considered separately; or at the very least each claim which is argued separately in the preceding sections of this brief should be considered separately. Argument: The fact that the claims use different formulations (as detailed above) and/or have been argued separately, shows that, if their patentability is not considered separately, any adverse decision would show that the limitations of some claims had been unfairly ignored.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

Respectfully submitted,
MUNCK BUTRUS, P.C.

Date: 6-4-2007

Daniel E. Venglarik
Registration No. 39,409

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *dvenglarik@munckbutrus.com*

Attorney for Applicant

DOCKET NO.: 00-BN-051 (STMI01-00051) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Anthony X. Jarvis, et al.
Serial No.:	09/751,372
Filed:	December 29, 2000
For:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX A -

Text of Claims on Appeal

1. (Previously Presented) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

2. (Original) The data processor as set forth in Claim 1 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation.

3. (Original) The data processor as set forth in Claim 2 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles.

4. (Previously Presented) The data processor as set forth in Claim 1 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation.

5. (Original) The data processor as set forth in Claim 4 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

6. (Previously Presented) The data processor as set forth in Claim 1 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation.

7. (Original) The data processor as set forth in Claim 6 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

8. (Original) The data processor as set forth in Claim 1 wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

9. (Original) The data processor as set forth in Claim 8 wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

10. (Previously Presented) A method of loading a first data value from a data cache into a target register of a plurality of registers, the method comprising the steps of:

determining if a pending instruction in an N-stage execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation;

in response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register;

in response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to the shifter circuit and shifting the first data value prior to loading the first data value into the target register; and

in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit.

11. (Original) The method as set forth in Claim 10 wherein the step of transferring the first data value requires two machine cycles during a load word operation.

12. (Original) The method as set forth in Claim 10 wherein the step of transferring the first data value requires three machine cycles during a load half-word operation.

13. (Original) The method as set forth in Claim 10 wherein the step of transferring the first data value requires three machine cycles during a load byte operation.

14. (Previously Presented) A processing system comprising:

a data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first

data value from said data cache directly to said target register without processing said first data value in said shifter circuit;

a memory coupled to said data processor; and

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

15. (Original) The processing system as set forth in Claim 14 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation.

16. (Original) The processing system as set forth in Claim 15 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles.

17. (Previously Presented) The processing system as set forth in Claim 14 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation.

18. (Original) The processing system as set forth in Claim 17 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

19. (Previously Presented) The processing system as set forth in Claim 14 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation.

20. (Original) The processing system as set forth in Claim 19 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

21. (Original) The processing system as set forth in Claim 14 wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

22. (Original) The processing system as set forth in Claim 21 wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

23. (Previously Presented) A processor, comprising:

a cache;

a plurality of registers;

a shifter circuit capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers; and

a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit.

24. (Previously Presented) The processor of Claim 23, wherein:

the data value is transferred from the cache to the target register via the bypass circuit during a load word operation; and

the data value is transferred from the cache to the target register via the shifter circuit during a load half-word operation or a load byte operation.

25. (Previously Presented) The processor of Claim 24, wherein:

the bypass circuit is capable of transferring the data value from the cache to the target register at an end of two machine cycles; and

the shifter circuit is capable of providing the modified data value to the target register at an end of three machine cycles.

26. (Previously Presented) The processor of Claim 23, wherein the bypass circuit comprises a multiplexer having a first input coupled to the cache and a second input coupled to the shifter circuit.

27. (Previously Presented) A method, comprising:

shifting, sign extending, or zero extending a first data value from a cache and providing a modified first data value to a first of a plurality of registers; and

transferring a second data value from the cache to a second of the plurality of registers without shifting, sign extending, or zero extending the second data value.

28. (Previously Presented) The method of Claim 27, wherein:

shifting, sign extending, or zero extending the first data value comprises shifting, sign extending, or zero extending the first data value in response to determining that a first pending instruction in a processor is a load byte operation or a load half-word operation; and

transferring the second data value comprises transferring the second data value to the second register in response to determining that a second pending instruction in the processor is a load word operation.

29. (Previously Presented) A system, comprising:

a processor comprising:

a cache;

a plurality of registers;

a shifter circuit capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers; and

a bypass circuit capable of transferring the data value from the cache to the target

register without processing the data value in the shifter circuit;

a memory coupled to the processor; and

a plurality of peripheral circuits capable of performing selected functions in association with the processor.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Anthony X. Jarvis, et al.
Serial No.:	09/751,372
Filed:	December 29, 2000
For:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX C -
Evidence Appendix

Not Applicable – No other evidence was entered.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Anthony X. Jarvis, et al.
Serial No.:	09/751,372
Filed:	December 29, 2000
For:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX D -
Related Proceedings Appendix

Not Applicable - To the best knowledge and belief of the undersigned attorney, there are none.

ATTORNEY DOCKET NO.: 00-BN-051 (STMI01-00051) PATENT
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	ANTHONY X. JARVIS, ET AL.
U. S. Serial No.	:	09/751,372
Filed	:	December 29, 2000
Title	:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Art Group Unit	:	2183
Examiner	:	Aimee J. Li

MAIL STOP APPEAL BRIEF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Appeal Brief;
3. Check in the amount of $500.00 for the Appeal Brief filing fee; and
5. Postcard receipt

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF-PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 4, 2007.

Date: 6/4/07 Kathy Cedar
Mailer

Date: 6-4-2007
Daniel E. Venglarik
Registration No. 39,409

P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *dvenglarik@munckbutrus.com*

DOCKET NO.: 00-BN-051 (STMI01-00051) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Anthony X. Jarvis, et al.
Serial No.:	09/751,372
Filed:	December 29, 2000
For:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX B -
Copy of Formal Drawings